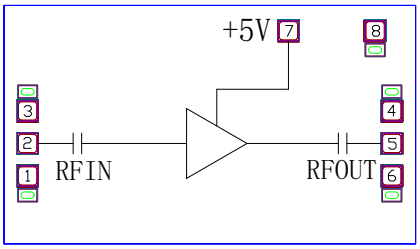
Features

·Freq: 22.0-30.0 GHz
·NF: 1.6dB
·Gain: 25dB
·Gain Flatness: ±0.4dB
·OP-1dB: 10.5 dBm
·Psat Satisfaction: 12 dBm
·OIP3: 21 dBm
·Supply Voltage: +5V/19mA
·50Ω Input/ Output
·Die Size: 1.9×1.1×0.1mm^3

Functional Diagram



General Description

The MC10037 is a Low Noise Amplifier which operates during 22.0-30.0 GHz.The amplifier Provides 25 dB of gain and 10.5 dBm of P-1dB Output power from a single bias supply of +5V/19mA with a noise figure of 1.6dB.

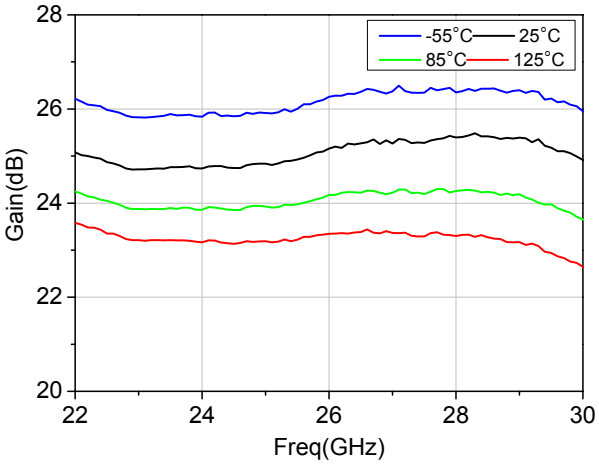
The Chip applies the on-chip metallization through-hole technology thus no need for additional grounding measures which makes it easy and convenient to use. The backside of the chip is metallized, suitable for conductive adhesive bonding or eutectic mounting process.

Electrical Specifications (TA=+25℃, 50Ω system, VD=+5V, Idd=19mA)

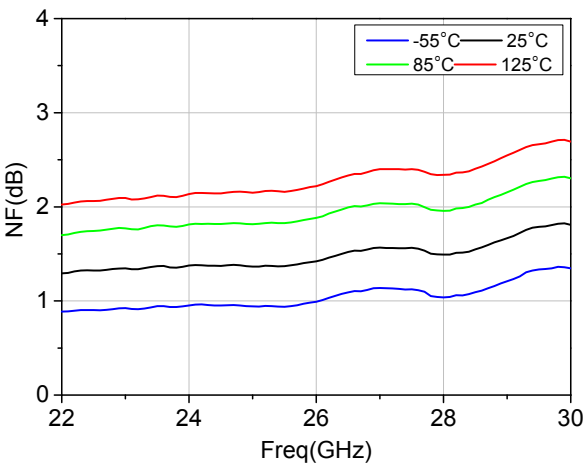
Parameter		Min.	Typ.	Max.	Unit
Frequency Range	Freq	22.0	-	30.0	GHz
Gain	Gain	-	25	-	dB
Gain Flatness	△ Gain	-	±0.4	-	dB
Noise Figure	NF	-	1.6	-	dB
Output P-1dB	P-1dB	-	10.5	-	dBm
Input Return Loss	IRL	-	-20	-	dB
Output Return Loss	ORL	-	-12	-	dB
Saturated Output Power	Psat	-	12	-	dBm
Output Third Order Intercept Point	OIP3	-	21	-	dBm
Quiescent Current	Idd	-	19	-	mA

[1] The chips are 100% DC and RF tested.

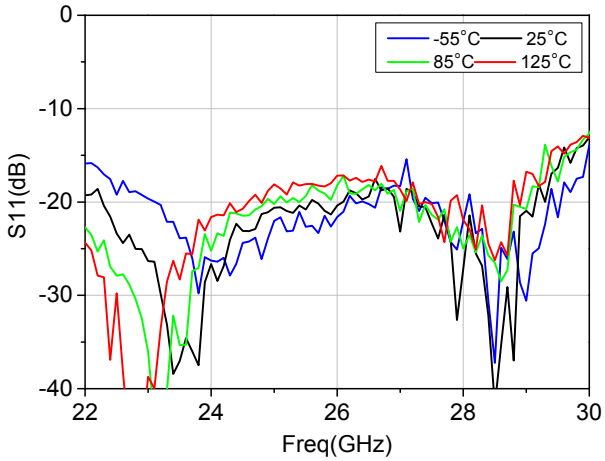
Typical Testing Characteristics



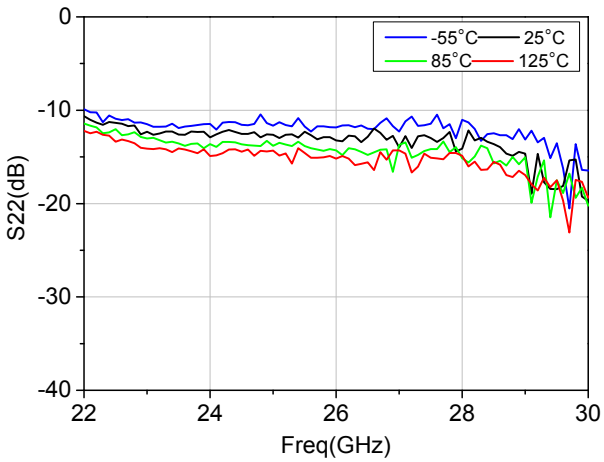
Gain vs Frequency



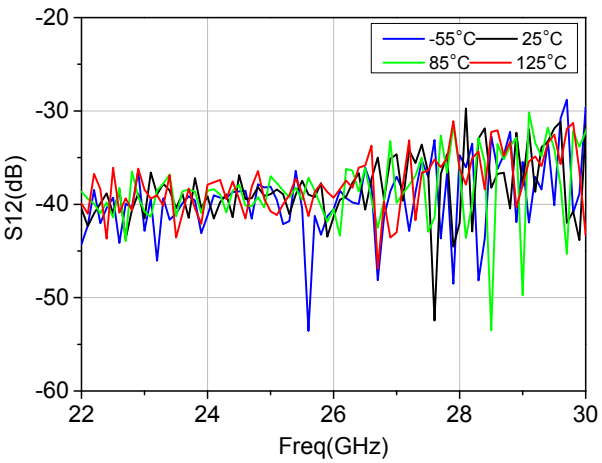
NF vs Frequency



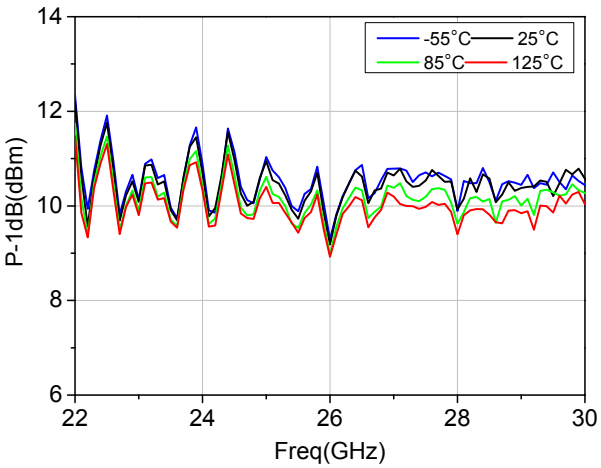
Input Return Loss vs Frequency



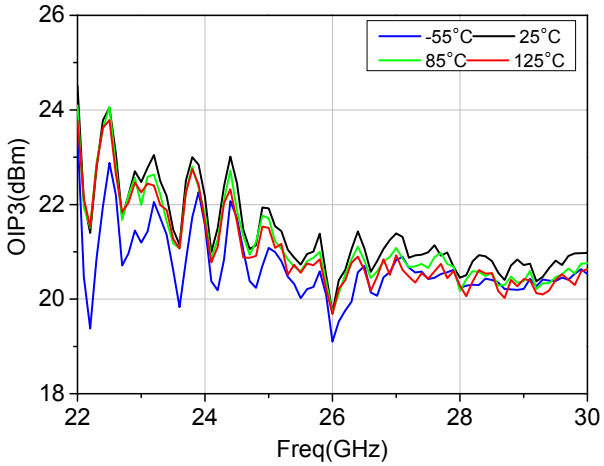
Output Return Loss vs Frequency



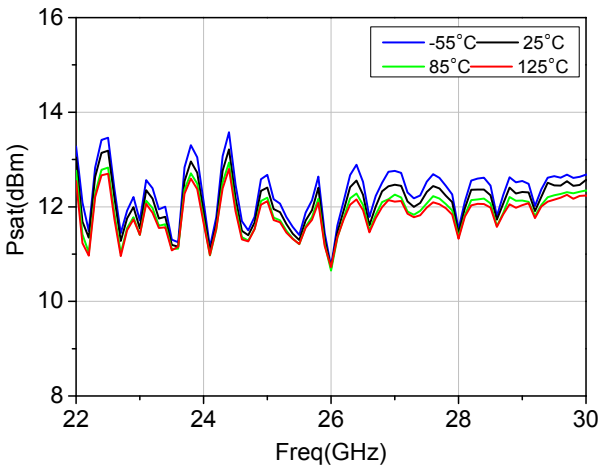
Reverse Isolation vs Frequency



Output P-1dB vs Frequency



OIP3 vs Frequency



Psat vs Frequency

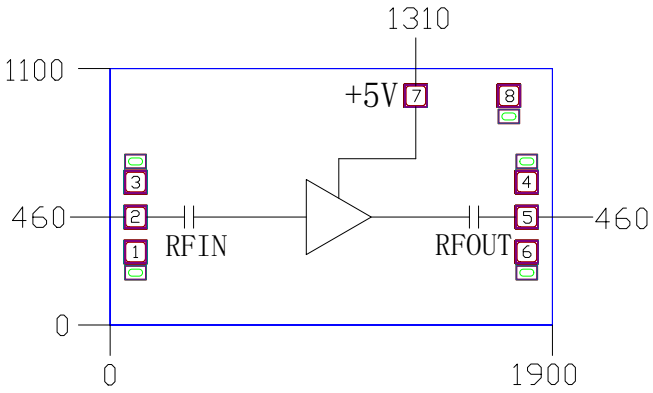
Absolute Maximum Ratings

Parameter Limits	Value
Input Power,50Ω	15dBm
Drain Bias Voltage VD	+6V
Storage Temperature	-65~+150℃
Operating Temperature	-55~+125℃
Mounting Temperature (30s, N_2 Protection)	300℃
Exceeding the above conditions may cause permanent damage to the chip	

This product is ESD(Electrostatic discharge) sensitive. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

·Assembling in a clean environment.
·Avoiding rapid temperature changes during the mounting process.
·Do not touch the surface or use dry/wet chemical methods to clean the surface
·2 bonding wires for input and output (in figure 八), the bonding wires should be as short as possible.
·Storing in a dry, N_2 protection environment.

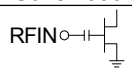
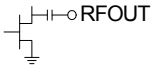
Outline Drawing



Notes:

1. Unit:μm
2. Back Side Metallization:Gold
3. Back side metal is ground
4. Bonding pad size: 100μm
5. Outline Dimensional Tolerance:±50 μm

Pad Descriptions

Pad No.	Function	Description	Interface Schematic
2	RFIN	RF signal input, 50Ω matched, with blocking capacitor inside	
5	RFOUT	RF Signal output, 50Ω matched, with blocking capacitor inside	
7	VD	Bias supplying voltage for the amplifier.External 100pF filter capacitor required	
1, 3, 4, 6, 8	GND	Grounding pad for probe test	
Die Bottom	GND	Die bottom must be connected to RF/DC ground	

Assembly Diagram