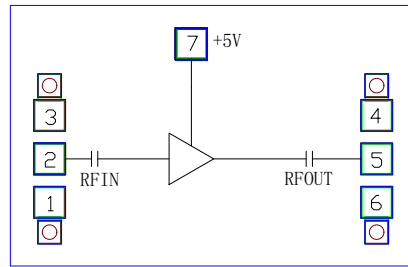


Features

- Freq: 2.0-14.0 GHz
- NF: 5.5 dB
- Gain: 17 dB
- Gain Flatness: ±0.6 dB
- OP-1dB: 15 dBm
- Psat Satisfaction: 18 dBm
- OIP3: 24 dBm
- Supply Voltage: +5V/55mA
- 50Ω Input/ Output
- Die Size: 1.4×0.9×0.1mm³

Functional Diagram



General Description

The MC1292 is a Driver Amplifier which operates during 2.0-14.0 GHz. The amplifier Provides 17 dB of gain and 15 dBm of P-1dB Output power from a single bias supply of +5V/55mA with a noise figure of 5.5 dB.

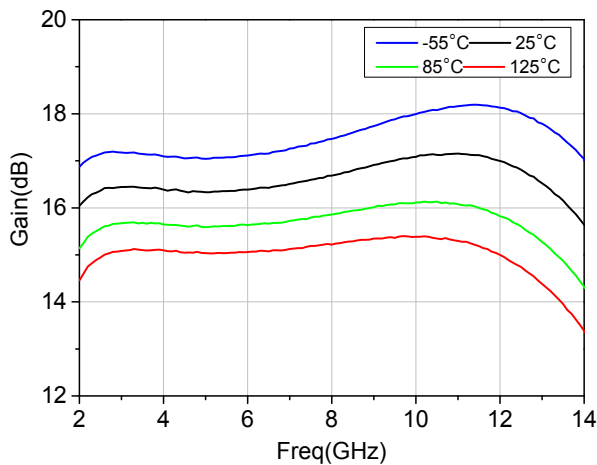
The Chip applies the on-chip metallization through-hole technology thus no need for additional grounding measures which makes it easy and convenient to use. The backside of the chip is metallized, suitable for conductive adhesive bonding or eutectic mounting process.

Electrical Specifications (T_A=+25°C, 50Ω system, V_D=+5V, I_{dd}=55mA)

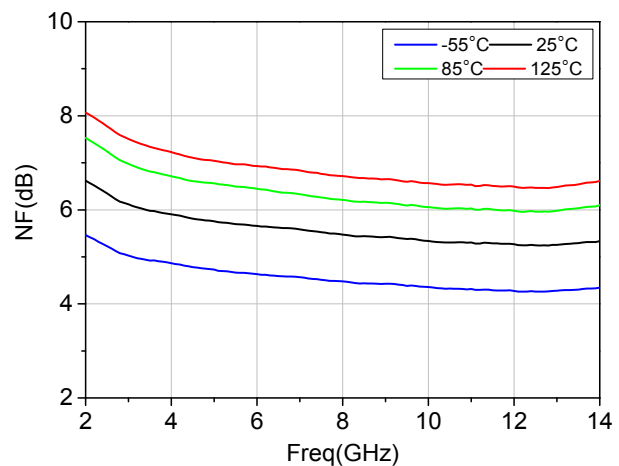
Parameter		Min.	Typ.	Max.	Unit
Frequency Range	Freq	2.0	-	14.0	GHz
Gain	Gain		17	-	dB
Gain Flatness	△ Gain	-	±0.6	-	dB
Noise Figure	NF	-	5.5	-	dB
Output P-1dB	P-1dB	-	15	-	dBm
Input Return Loss	IRL	-	-20	-	dB
Output Return Loss	ORL	-	-20	-	dB
Saturated Output Power	Psat	-	18	-	dBm
Output Third Order Intercept Point	OIP3	-	24	-	dBm
Quiescent Current	I _{dd}	-	55	-	mA

[1] The chips are 100% DC and RF tested.

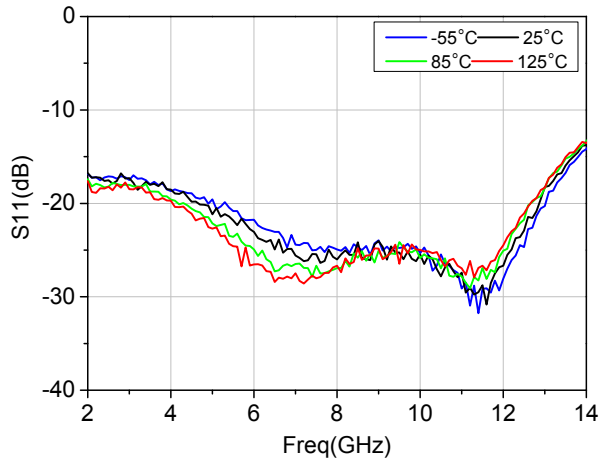
Typical Testing Characteristics



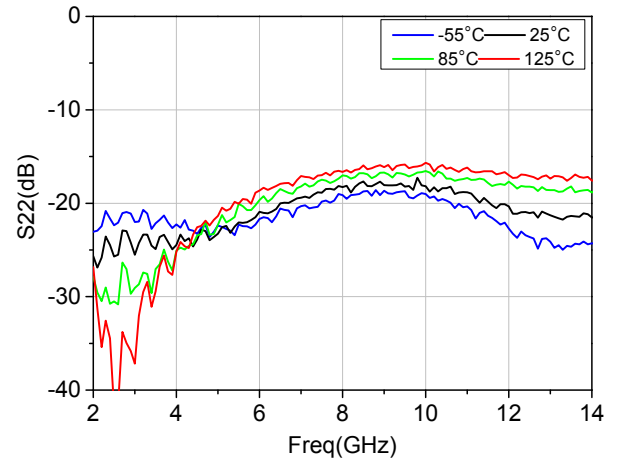
Gain vs Frequency



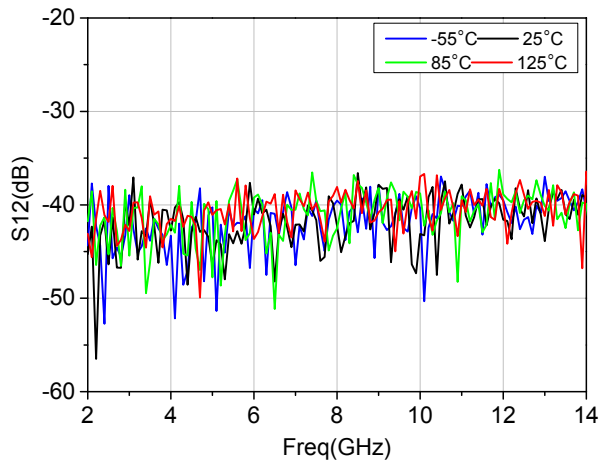
NF vs Frequency



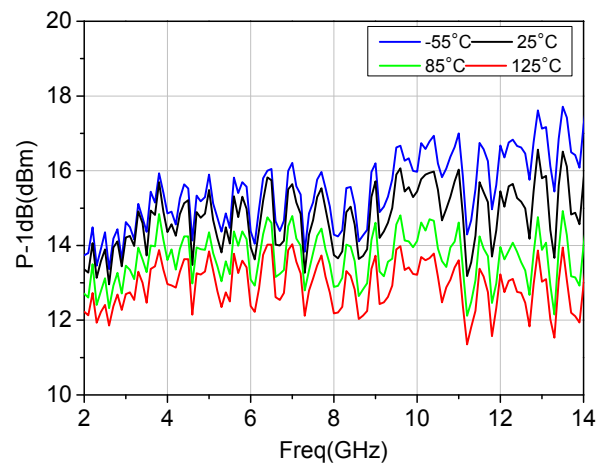
Input Return Loss vs Frequency



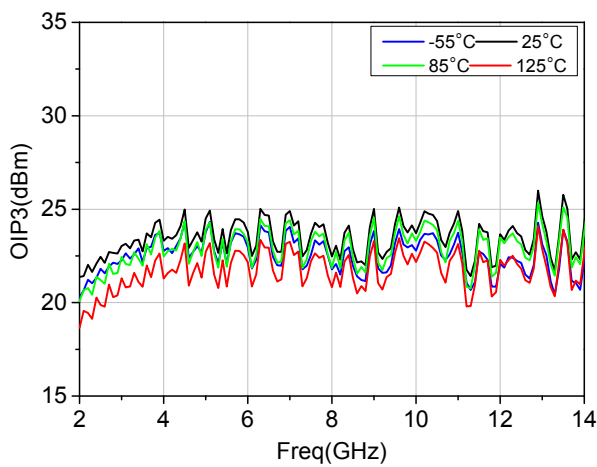
Output Return Loss vs Frequency



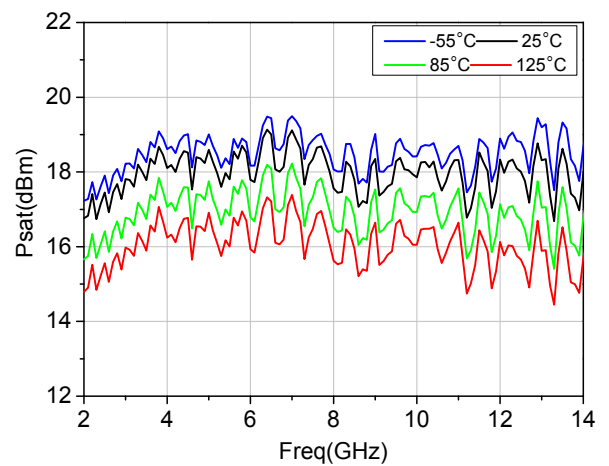
Reverse Isolation vs Frequency



Output P-1dB vs Frequency



OIP3 vs Frequency

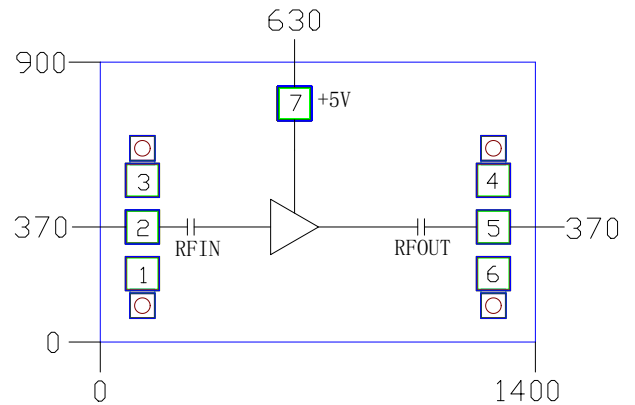


Psat vs Frequency

Absolute Maximum Ratings

Parameter Limits	Value
Input Power, 50Ω	15dBm
Drain Bias Voltage VD	+6V
Storage Temperature	-65~+150°C
Operating Temperature	-55~+125°C
Mounting Temperature (30s, N ₂ Protection)	300°C
Exceeding the above conditions may cause permanent damage to the chip	

Outline Drawing



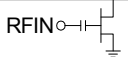
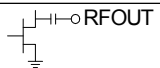



This product is ESD(Electrostatic discharge) sensitive. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

- Assembling in a clean environment.
- Avoiding rapid temperature changes during the mounting process.
- Do not touch the surface or use dry/wet chemical methods to clean the surface
- 2 bonding wires for input and output (in figure 八), the bonding wires should be as short as possible.
- Storing in a dry, N₂ protection environment.

Notes:

1. Unit: μm
2. Back Side Metallization: Gold
3. Back side metal is ground
4. Bonding pad size: 100μm
5. Outline Dimensional Tolerance: ±50 μm

Pad Descriptions

Pad No.	Function	Description	Interface Schematic
2	RFIN	RF signal input , 50Ω matched, without blocking capacitor inside	
5	RFOUT	RF Signal output, 50Ω matched, blocking capacitor and chocking inductance required	
7	VD	Bias supplying voltage for the amplifier. External 100pF filter capacitor required	
1, 3, 4, 6	GND	Grounding pad for probe test	
Die Bottom	GND	Die bottom must be connected to RF/DC ground	

Assembly Diagram

