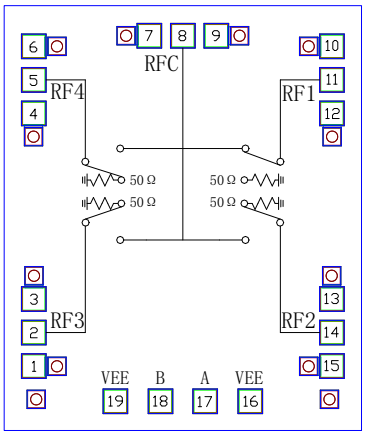
Features

·Freq: DC-20.0 GHz
·Insertion Loss: 1.8 dB
·Isolation: 50 dB
·Input Return Loss: -18 dB
·On-state output return loss: -19 dB
·Off-state output return loss: -26 dB
·50Ω Input/ Output
·Die Size: 1.6×1.9×0.1mm^3

Functional Diagram



General Description

The MC15120 is a nonreflective SP4T switch which operates during DC-20.0 GHz.The typical insertion loss is 1.8dB and the isolation is 50dB. With 0V/+3.3V logic control, an external -5V power bias is required, the typical bias current is 8mA, and the switching speed is less than 50ns.

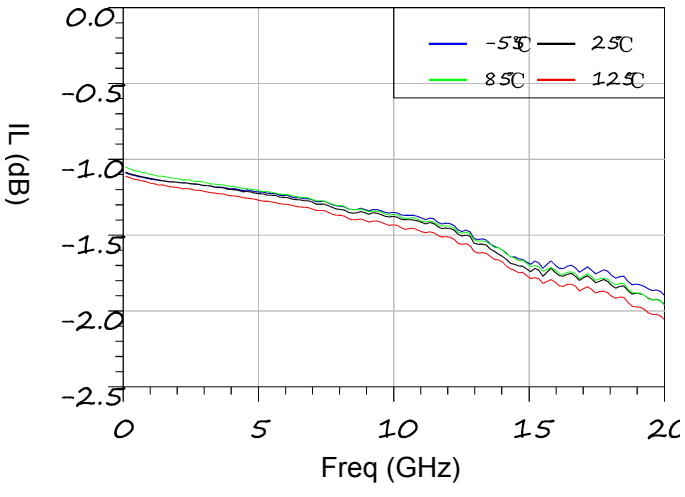
The Chip applies the on-chip metallization through-hole technology thus no need for additional grounding measures which makes it easy and convenient to use. The backside of the chip is metallized, suitable for conductive adhesive bonding or eutectic mounting process.

Electrical Specifications (TA=+25℃, 50Ω system,0V/+3.3V Control (0/+5V Control Compatible))

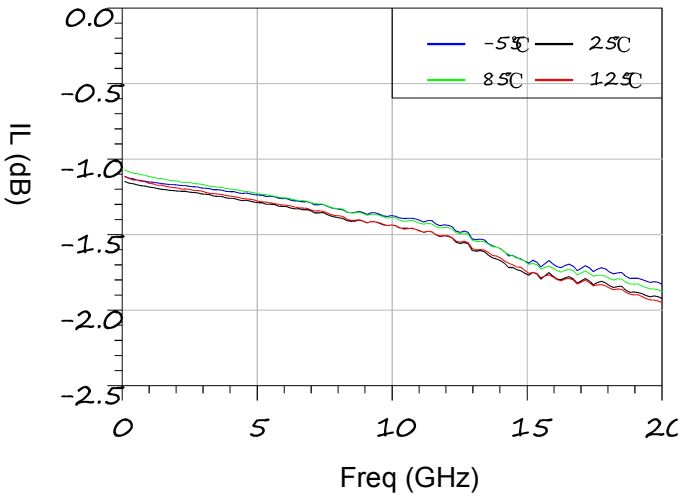
Parameter		Min.	Typ.	Max.	Unit
Frequency Range	Freq	DC	-	20.0	GHz
Insertion Loss	IL	-	1.8	-	dB
Isolation	ISO	-	50	-	dB
Input Return Loss	IRL	-	-18	-	dB
On-state output return loss	ORL	-	-19	-	dB
Off-state output return loss	ORL	-	-26	-	dB
Switching time	T	-	-	50	ns
Bias current	I	-	8	-	mA

[1] The chips are 100% DC and RF tested.

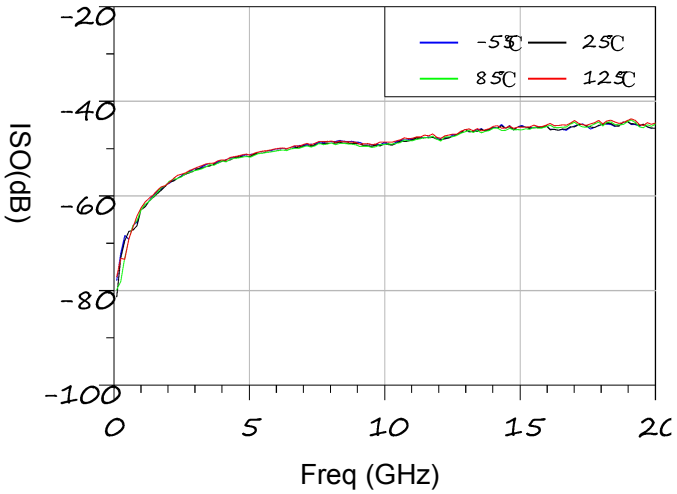
Typical Testing Characteristics



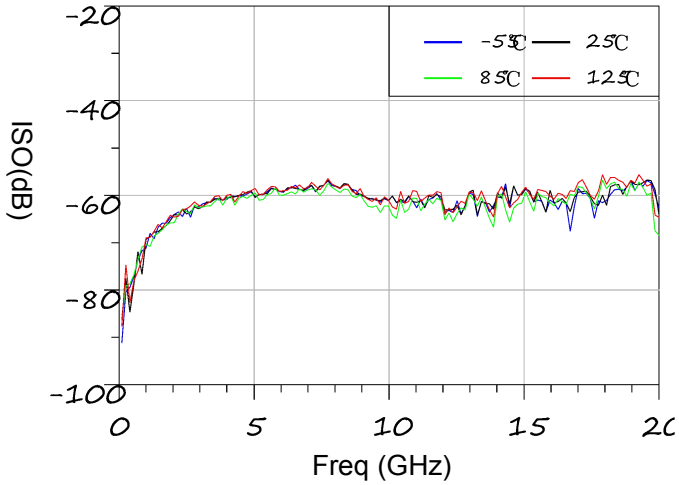
RF1/RF4 on-state insertion loss vs Frequency



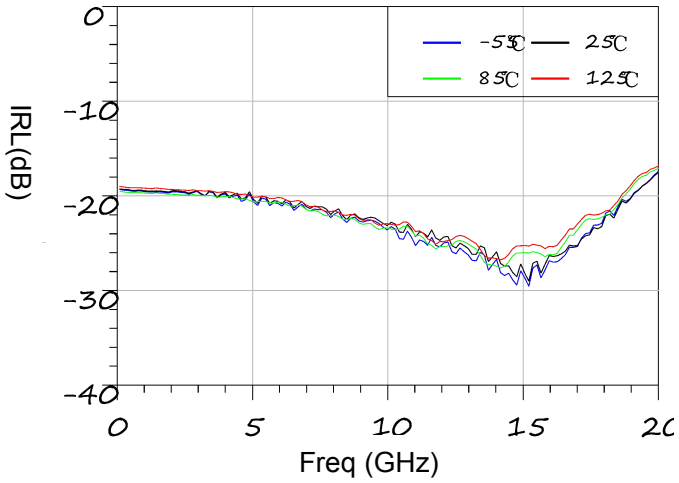
RF2/RF3 on-state insertion loss vs Frequency



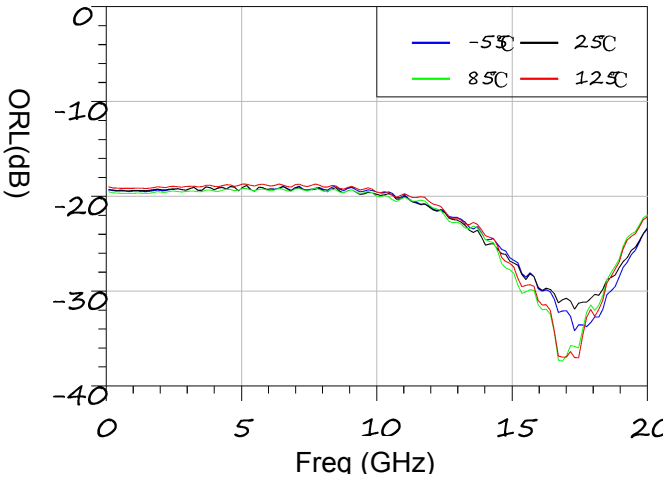
RF1/RF4 off-state insertion loss vs Frequency



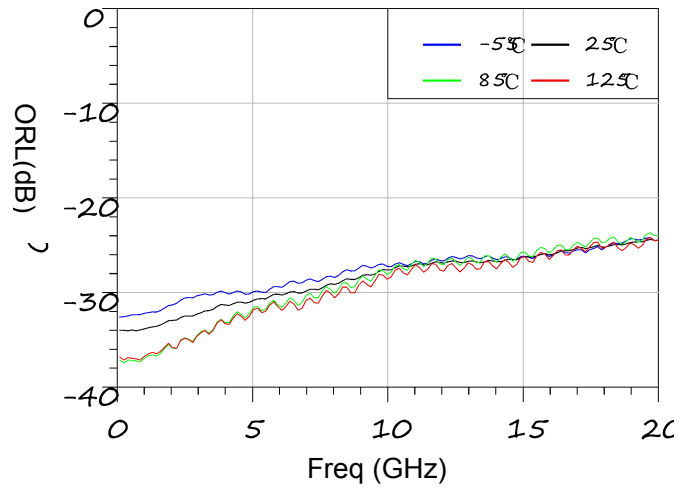
RF2/RF3 off-state insertion loss vs Frequency



Input Return Loss vs Frequency



on-state output return loss vs Frequency



off-state output return loss vs Frequency

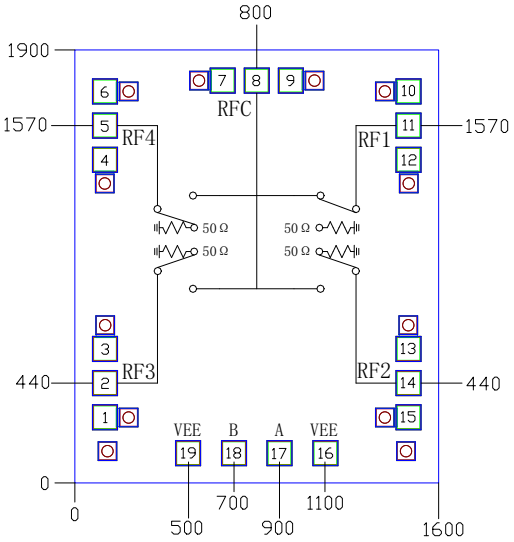
Absolute Maximum Ratings

Parameter Limits	Value
Input Power,50Ω	23dBm
Control Voltage	0V~+5V
Storage Temperature	-65~+150℃
Operating Temperature	-55~+125℃
Mounting Temperature (30s, N_2 Protection)	300℃
Exceeding the above conditions may cause permanent damage to the chip	

This product is ESD(Electrostatic discharge) sensitive. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

- Assembling in a clean environment.
- Avoiding rapid temperature changes during the mounting process.
- Do not touch the surface or use dry/wet chemical methods to clean the surface
- 2 bonding wires for input and output (in figure 八), the bonding wires should be as short as possible.
- Storing in a dry, N_2 protection environment.

Outline Drawing



Notes:

1. Unit:μm
2. Back Side Metallization:Gold
3. Back side metal is ground
4. Bonding pad size: 100μm
5. Outline Dimensional Tolerance:±50 μm

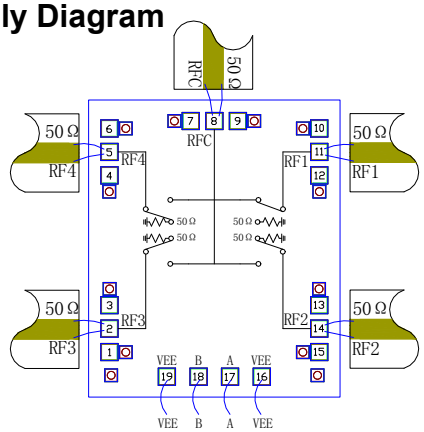
Pad Descriptions

Pad No.	Function	Description	Interface Schematic
8	RFC	RF signal input, 50Ω matched, without blocking capacitor inside	RFIN
2, 5, 11, 14	RFOUT	RF Signal output, 50Ω matched, without blocking capacitor inside	RFOUT
17, 18	A, B	DC control signal, 0V/+3.3V voltage matched	A
16, 19	VEE	Bias voltage, these two VEEs are connected internally, connect either of them while use	VEE
1, 3, 4, 6, 7, 9, 10, 12, 13, 15	GND	Grounding pad for probe test	GND
Die Bottom	GND	Die bottom must be connected to RF/DC ground	GND

Control Voltage Range

Typ.	Control Voltage Range
0V	0V~+0.5V
+3.3V	+3V~+5V

Assembly Diagram



Control Logic

Power Voltage	Control Input		On-off state			
VE	A	B	RF1	RF2	RF3	RF4
-5V	0V	0V	ON	OFF	OFF	OFF
-5V	3.3V	0V	OFF	ON	OFF	OFF
-5V	0V	3.3V	OFF	OFF	ON	OFF
-5V	3.3V	3.3V	OFF	OFF	OFF	ON