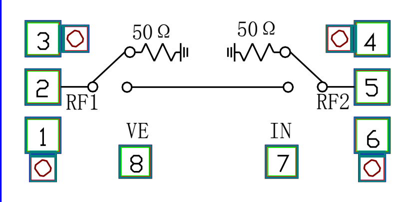
Key features

- Freq: DC-20.0GHz
- Insertion Loss:1.4dB
- Isolation:55dB
- On-Stage RF1 Return Loss:-18dB
- Off-Stage RF1 Return Loss:-15dB
- On-Stage RF2 Return Loss:-18dB
- Off-Stage RF2 Return Loss:-15dB
- 50Ω Input/Output
- Size:1.3×0.65×0.1mm3

Functional Diagram



Description

MC15101 is an absorptive single-pole single-throw switch chip, working at DC-20.0GHz, typical insertion loss 1.4dB, typical isolation 55dB, adopts 0V/+3.3V logic control, requires an external -5V power bias, typical bias Current 2mA, switching speed is less than 50ns.

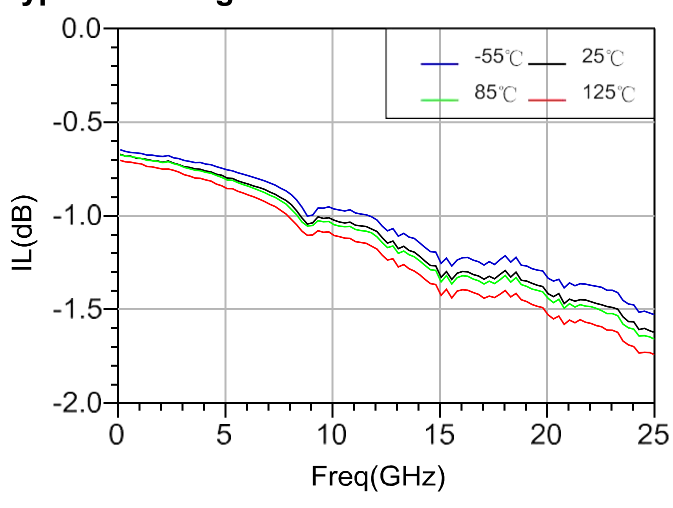
The switch chip adopts an on-chip metallized through-hole process without additional grounding measures, and is simple and convenient to use; the back of the chip is metallized, which is suitable for conductive adhesive bonding or eutectic mounting process.

Electrical Specifications (TA=+25℃, 50Ω system, 0V/+3.3V Control(Compatible 0/+5V Control))

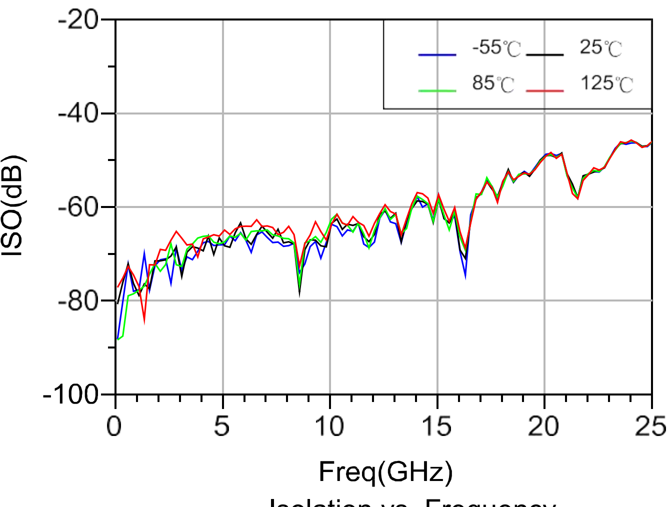
Parameters	Function	Min.	Typ.	Max.	Units
Working Frequency	Freq	DC	-	20.0	GHz
Insertion Loss	IL	-	1.4	-	dB
Isolation	ISO	-	55	-	dB
On-Stage RF1 Return Loss	RF1RL	-	-18	-	dB
Off-Stage RF1 Return Loss	RF1RL	-	-15	-	dB
On-Stage RF2 Return Loss	RF2RL	-	-18	-	dB
Off-Stage RF2 Return Loss	RF2RL	-	-15	-	dB
Switching time	T	-	-	50	ns
Bias current	I	-	2	-	mA

[1] The chips are 100% DC and RF tested.

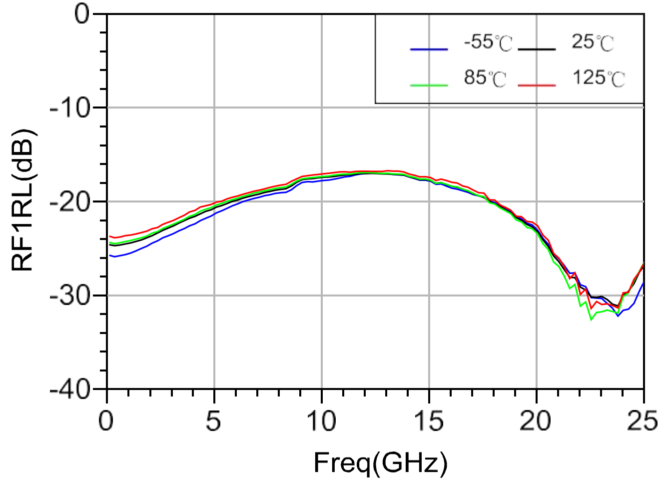
Typical Testing Characteristics



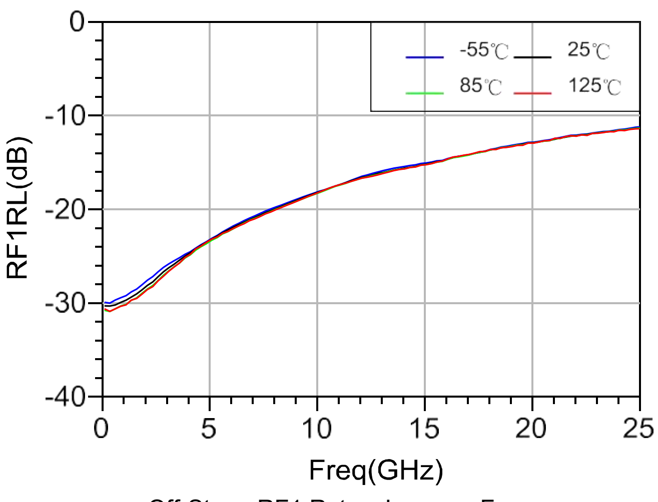
Insertion Loss vs Frequency



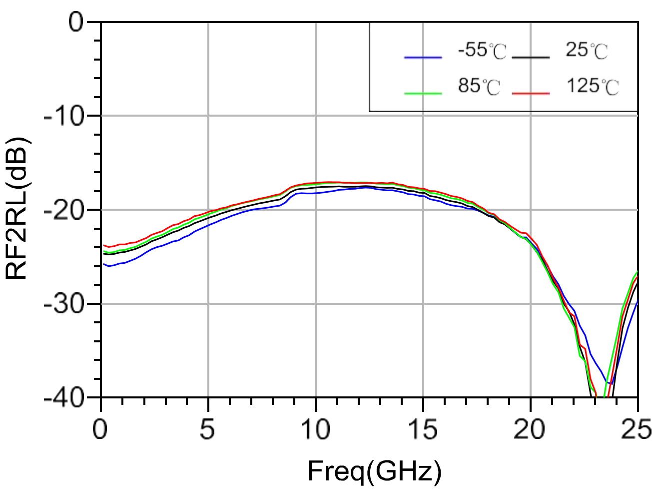
Isolation vs Frequency



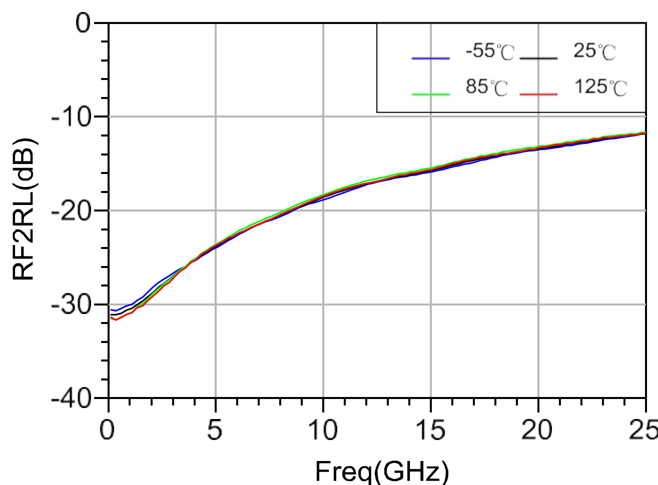
On-Stage RF1 Return Loss vs Frequency



Off-Stage RF1 Return Loss vs Frequency



On-Stage RF2 Return Loss vs Frequency



Off-Stage RF2 Return Loss vs Frequency

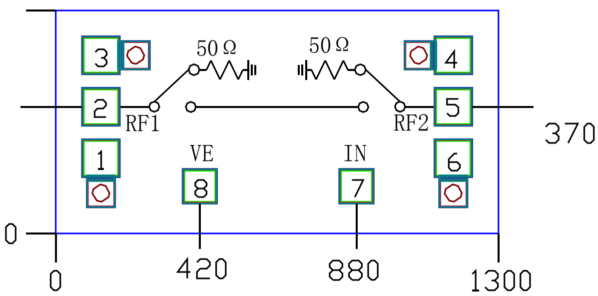
Absolute Maximum Ratings

Parameter Limits	Value
Pin,50Ω	23dBm
Control voltage range	0V~+5V
Storage Temperature	-65~+150℃
Operating Temperature	-55~+125℃
Mounting Temperature (30s,N_2 Protection)	300℃
Exceeding the above conditions may cause permanent damage to the chip.	

This product is ESD sensitive. Proper ESD precautions shall be taken to avoid performance degradation or loss of functionality.

- Assembling in a clean environment.
- Avoiding rapid temperature changes during the mounting process.
- Do not touch the surface or use dry /wet chemical methods to clean the surface.
- Using 2 bonding wires(shaped as figure eight for input and output,the bonding wires should be as short as possible
- Storing in a dry,N2 protection environment.

Outline Drawing



Notes:

1. Unit:μm
2. Back side Metallization:Gold
3. Back side metal is ground
4. Bonding pas size:100μm
5. Outline Dimensional Tolerance:±50 μm

Pad Description

Pad No.	Function	Description	Interface Schematic
2	RF1	RF signal input/output terminal, external 50Ω system, no DC blocking capacitor inside the chip	RF1
5	RF2	RF signal input/output terminal, external 50Ω system, no DC blocking capacitor inside the chip	RF2
7	IN	DC control signal, external 0V/+3.3V voltage	IN
8	VE	Bias voltage terminal, external -5V	VE
1, 3, 4, 6	GND	Ground pressure pad for probe test	GND
Die bottom	GND	The bottom of the chip needs to be in good contact with the RF and DC ground	GND

Control voltage range

Typical Value	Control Voltage Range
0V	0V~+0.5V
+3.3V	+3V~+5V

Electrical Specifications:

Voltage	Control Input	Stage
VE	IN	
-5V	0V	ON
-5V	+3.3V	OFF

Assembly Diagram